Understanding Pipelined ADCs

This article explains the architecture and operation of pipelined analog-to-digital converters (ADCs). It discusses key performance characteristics of pipeline ADCs such as architecture, latency, digital error correction, component accuracy, and digital calibration. It also has a brief comparison versus other data converter architectures.

The pipelined analog-to-digital converter (ADC) has become the most popular ADC architecture for sampling rates from a few megasamples per second (MS/s) up to 100MS/s+, with resolutions from 8 bits at the faster sample rates up to 16 bits at the lower rates. These kinds of resolutions and sampling rates cover a wide range of applications, including CCD imaging, ultrasonic medical imaging, digital receiver, base station, digital video (for example, HDTV), xDSL, cable modem, and fast Ethernet.

Lower-sampling-rate applications are still the domain of the successive approximation register (SAR) and integrating architectures (and more recently oversampling/sigma-delta ADCs), whereas the highest sampling rates (a few hundred MS/s or higher) are still obtained using flash ADCs and their variants. However, it is safe to say that pipelined ADCs of various forms have improved greatly in speed, resolution, dynamic performance, and low power in recent years.

Pipelined ADC Architecture

Figure 1 shows a possible block diagram of a 12-bit pipelined ADC.

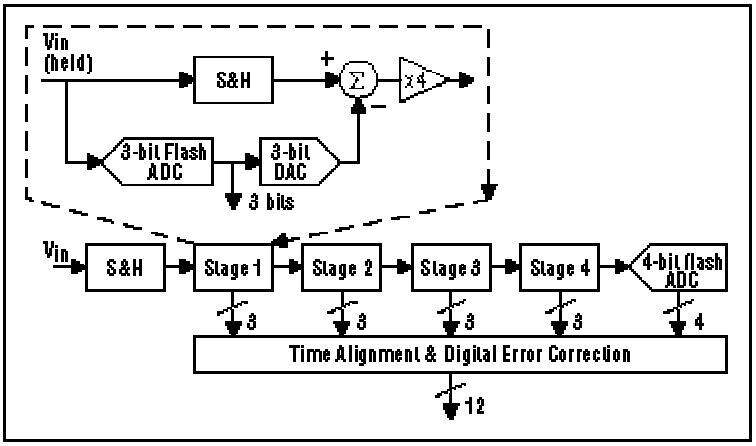

Figure 1. Pipelined ADC with four 3-bit stages (each stage resolves 2 bits)

Here, the analog input V_{IN} is first sampled and held steady by a sample-and-hold (S&H), while the flash ADC in stage one quantizes it to 3 bits. The 3-bit output is then fed to a 3-bit DAC (accurate to about 12 bits), and the analog output is subtracted from the input. This "residue" is then gained up by a factor of 4 and fed to the next stage (stage two). This gained-up residue continues through the pipeline, providing 3 bits per stage until it reaches the 4-bit flash ADC, which resolves the last 4LSB bits. Because the bits from each stage are determined at different points in time, all the bits corresponding to the same sample are time-aligned with shift registers before being fed to the digital-error-correction logic. Note that as soon as a certain stage finishes processing a sample, determining the bits and passing the residue to the next stage, it can start processing the next sample due to the sample-and-hold embedded within each stage. This pipelining action accounts for the high throughput.

Latency

Because each sample has to propagate through the entire pipeline before all its associated bits are available for combining in the digital-error-correction logic, data latency is associated with pipelined ADCs. In the example in Figure 1, this latency is about three cycles (see Figure 2).

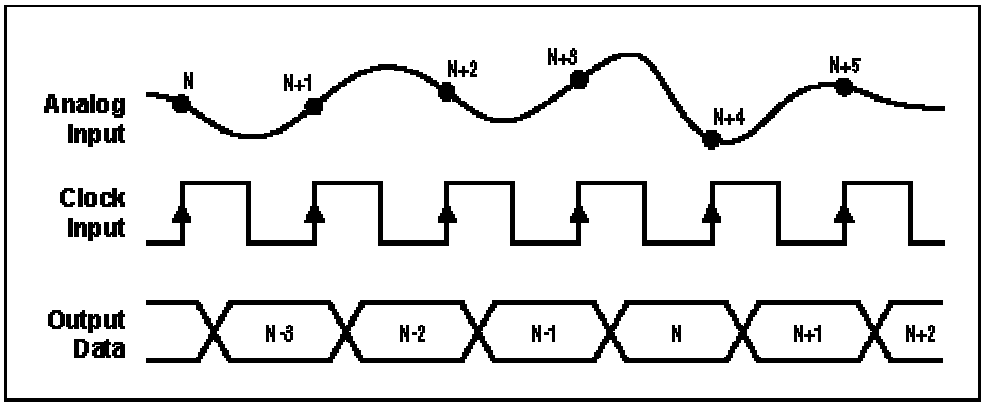

Figure 2. Data latency in a pipelined ADC

Digital Error Correction

Most modern pipelined ADCs employ a technique called "digital error correction" to greatly reduce the accuracy requirement of the flash ADCs (and thus the individual comparators). In Figure 1, notice that the 3-bit residue at the summation-node output has a dynamic range one-eighth that of the original stage-one input (V_{IN}), yet the subsequent gain is only 4. Therefore, the input to stage two occupies only half the range of the 3-bit ADC in stage two (that is, when there is no error in the first 3-bit conversion in stage one).

If one of the comparators in the first 3-bit flash ADC has a significant offset, when an analog input close to the trip point of this comparator is applied, an incorrect 3-bit code and thus an incorrect 3-bit DAC output would result, producing a different residue. However, it can be proven that, as long as this gained-up residue doesn't over-range the subsequent 3-bit ADC, the

LSB code generated by the remaining pipeline when added to the incorrect 3-bit MSB code will give the correct ADC output code. The implication is that none of the flash ADCs in Figure 1 has to be as accurate as the entire ADC. In fact, the 3-bit flash ADCs in stages one through four require only about 4 bits of accuracy.

The digital error correction will not correct for errors made in the final 4-bit flash conversion. However, any error made here is suppressed by the large (4^4) cumulative gain preceding the 4-bit flash, requiring the final stage to be only more than 4-bits accurate.

In the example in Figure 1, although each stage generates 3 raw bits, because the interstage gain is only 4, each stage (stages one to four) effectively resolves only 2 bits. The extra bit is simply to reduce the size of the residue by one half, allowing extra range in the next 3-bit ADC for digital error correction, as mentioned above. This is called "1-bit overlap" between adjacent stages. The effective number of bits of the entire ADC is therefore 2 + 2 + 2 + 2 + 4 = 12 bits.

Component Accuracy

Digital error correction does not correct gain or linearity errors in the individual DAC and gain amplifiers. In particular, the front-end S&Hs and DAC need about 12-bit accuracy, whereas the components in subsequent stages require less accuracy (for example, 10-bit for stage two, 8-bit for stage three, and so forth) because their error terms are divided down by the preceding interstage gain(s). This fact is often exploited to further save power by making the pipelined stages progressively smaller.

In most pipelined ADCs designed with CMOS or BiCMOS technology, the S&H, the DAC, the summation node, and the gain amplifier are usually implemented as a single *switched-capacitor* circuit block called a multiplying DAC (MDAC). The major factor limiting MDAC accuracy is the inherent capacitor mismatch. A purely bipolar implementation would be more complicated and would suffer mainly from resistor mismatch in the current source DAC and the interstage gain amplifier.

In general, for about 12 bits of accuracy or higher, some form of capacitor/resistor trimming or digital calibration is required, especially for the first couple of stages.

Digital Calibration

The MAX1200/MAX1201/MAX1205 family * (16-bit 1MS/s, 14-bit 1MS/s and 2MS/s ADC) employs digital calibration to ensure its excellent accuracy and dynamic performance. The MAX1200 family is a CMOS pipelined ADC with four 4-bit stages (with 1-bit overlap) and a 5-bit flash ADC at the end, giving a total of 3 + 3 + 3 + 3 + 5 = 17 raw bits (see Figure 3). The extra 1 to 3 bits are required by the digital calibration to quantize the error terms to greater accuracy than the ADC itself and are discarded to give either 14 bits or 16 bits overall.

Calibration starts from the MDAC in the third stage; beyond the third stage the MDAC error terms are small enough that calibration is not needed. The third-stage output is digitized by the remaining pipelined ADC, and the error terms are stored in on-chip RAM. Once the third MDAC is calibrated, it can be used to calibrate the second MDAC in a similar fashion. Likewise, once the second and third MDAC are calibrated, they are used to calibrate the first MDAC. Averaging is used (especially in the first and second MDAC) to ensure that the

calibration is noise-free. During normal conversions, those error terms are recalled from the RAM and are used to adjust the outputs from the digital-error-correction logic.

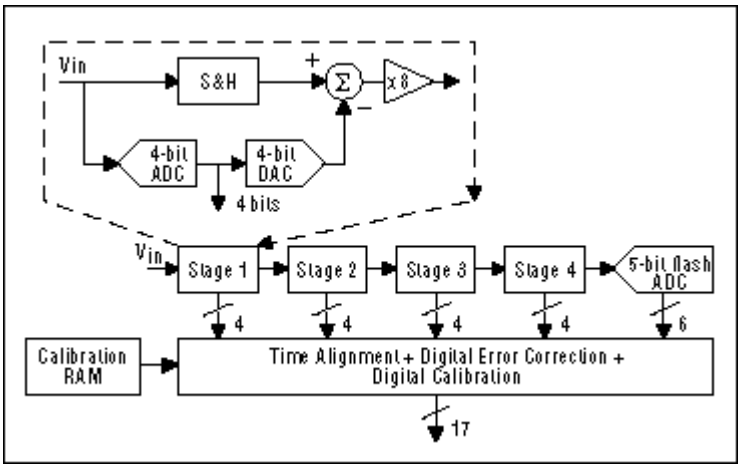

Figure 3. MAX1200 pipelined ADC architecture

Different Variations

From the example in Figure 1, it is obvious that, depending on how many bits each stage resolves, the number of bits in the LSB flash ADC, and whether digital calibration or trimming is used to improve the accuracy of the first couple of stages, there can be many variations of pipelined ADC. This partition of bits per stage is determined in part by the target sampling rate and resolution. In general, higher-speed CMOS pipelined ADCs tend to favor a lower number of bits per stage (as low as just 1 bit per stage so that the interstage gain is only 2), because it is difficult to realize wideband amplifiers of very high gain in CMOS. Lower-sampling-rate CMOS pipelined ADCs and bipolar pipelined ADCs (even those with a very high sampling rate) tend to favor more bits per stage. This also results in less data latency.

The CMOS MAX1425/MAX1426 (10-bit 10MS/s and 20MS/s) family uses the popular 1.5 bit per stage architecture, with each stage resolving only 1 bit with "0.5-bit overlap." Each 1.5-bit stage has a 1.5-bit flash ADC (only two comparators), versus a full 2-bit flash ADC. It can be shown that, with digital error correction, this works the same way as a regular MDAC stage with 2-bit flash ADC and DAC. These converters achieve a high SNR of 59dB with 10MHz analog inputs sampled at 20MS/s.

The MAX1444/MAX1446/MAX1448/MAX1449 family (10-bit 40/60/80/105MS/s) is the latest generation of high-speed very-low-power 10-bit ADC employing the 1.5 bit per stage architecture. These CMOS devices incorporate wideband low-distortion track-and-hold amplifiers to ensure excellent dynamic performance throughout and beyond the Nyquist band. Undersampling, popular in digital receiver design, is possible with these families.

Pipelined ADC versus Other ADCs

Versus SAR

In a successive approximation register (SAR) ADC, the bits are decided by a single high-speed, high-accuracy comparator bit by bit, from the MSB down to the LSB, by comparing the analog input with a DAC whose output is updated by previously decided bits and *successively approximates* the analog input. This serial nature of SAR limits its operating speed to no more than a few MS/s, and still slower for very high resolutions (14 to 16 bits). A pipelined ADC, however, employs a parallel structure in which each stage works on 1 to a few bits (of successive samples) concurrently. Although there is only one comparator in a SAR, this comparator has to be fast (clocked at approximately *the number of bits x the sample rate*) and as accurate as the ADC itself. In contrast, none of the comparators inside a pipelined ADC needs this kind of speed or accuracy.

However, a pipelined ADC generally takes up significantly more silicon area than an equivalent SAR. A SAR also displays a latency of only one cycle (one cycle = $1/F_{sample}$), versus about three or more cycles in a typical pipeline. Like a pipeline, a SAR with more than 12 bits of accuracy usually requires some form of trimming or calibration.

Versus Flash

Despite the inherent parallelism, a pipelined ADC still requires accurate analog amplification in DACs and interstage gain amplifiers, and thus significant linear settling time. A purely flash ADC, on the other hand, has a large bank of comparators, each consisting of wideband, low-gain preamps followed by a latch. The preamps, unlike those amplifiers in a pipelined ADC, need to provide gains that don't even have to be linear or accurate—meaning, only the comparators' trip points have to be accurate. As a result, a pipelined ADC cannot match the speed of a well-designed flash ADC.

Although extremely fast 8-bit flash ADCs (or their folding/interpolation variants) exist with sampling rates as high as 1.5GS/s (for example, the MAX104/MAX106/MAX108), it is much harder to find a 10-bit flash, while 12-bit (or above) flash ADCs are not commercially viable products. This is simply because in a flash the number of comparators goes up by a factor of 2 for every extra bit of resolution, and at the same time each comparator has to be twice as accurate. In a pipeline, however, to a first order the complexity only increases linearly with the resolution, not exponentially.

At sampling rates obtainable by both a pipeline and a flash, a pipelined ADC tends to have much lower power consumption than a flash. A pipeline also tends to be less susceptible to comparator metastability. Comparator metastability in a flash can lead to *sparkle-code* errors (a condition in which the ADC provides unpredictable, erratic conversion results).

Versus the Sigma-Delta Converter

Traditionally, oversampling/sigma-delta-type converters commonly used in digital audio have a limited bandwidth of about 22kHz or so. But recently some high-bandwidth sigma-delta-type converters have reached a bandwidth of 1MHz to 2MHz with 12 to 16 bits of resolution. These are usually very-high-order sigma-delta modulators (for example, fourth or even higher)

incorporating a multi-bit ADC and multi-bit feedback DAC, and their main applications are in ADSL. Sigma-delta converters have the innate nature of requiring no special trimming/calibration, even for 16 to 18 bits of resolution. They also require no steep rolling-off anti-alias filter at the analog inputs, because the sampling rate is much higher than the effective bandwidth; the backend digital filters take care of it. The oversampling nature of the sigma-delta converter also tends to "average out" any system noise at the analog inputs.

However, sigma-delta converters trade speed for resolution. The need to sample many times (for example, at least 16 times, but often much higher) to produce one final sample causes the internal analog components in the sigma-delta modulator to operate much faster than the final data rate. The digital decimation filter is also nontrivial to design and takes up a lot of silicon area. The fastest, high-resolution sigma-delta-type converters are not expected to have more than a few MHz of bandwidth in the near future. Like pipelined ADCs, sigma-delta converters also have latency.

Versus Half (Two-Step) Flash

A two-step flash can be generalized as a two-stage pipeline. However, as the number of bits goes up (for example, 12 bits or higher) with digital error correction, each stage would need to incorporate a 6- to 7-bit flash ADC. The interstage gain amplifier would also need very high gain. Therefore, for higher resolution, it is wiser to use more than two stages.

Conclusion

The pipelined ADC is the architecture of choice for sampling rates from a few MS/s up to 100MS/s+. Complexity goes up only linearly (not exponentially) with the number of bits, providing converters with high speed, high resolution, and low power at the same time. They are very useful for a wide range of applications, most notably in the digital communication area, where a converter's dynamic performance is often more important than traditional DC specifications like differential nonlinearity (DNL) and integral nonlinearity (INL). Their data latency is of little concern in most applications.

Maxim continues to develop new converters that will enhance its portfolio of pipelined ADCs. These include the soon-to-be-announced high-performance MAX1420/MAX1421/MAX1422, which are 12-bit 20/40/60MS/s converters. Maxim's pipelined ADCs nicely complement its ADC families designed with other architectures.

*For more details, please refer to the article "Pipeline ADCs Come of Age."

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